because it is clear from the Office Action that the Examiner understands that the originally claimed phrase "material layer" refers to a layer formed on the semiconductor wafer (see Office Action, page 2, lines 13-18). Applicants submit that the proposed amendments to claims 6 and 8 do not change the scope of these claims or raise new issues that require additional consideration.

Based on the foregoing, Applicants request that the rejection of claims 6-10 under 35 U.S.C. § 112, second paragraph be withdrawn and the claims allowed.

Applicants respectfully traverse the rejections of claims 1-10 under 35 U.S.C. § 103(a) because Ye et al. and Lau et al., alone or in combination, fail to teach, or suggest all of the elements of these claims. Further, Applicants respectfully traverse the rejections of claims 1-10 under 35 U.S.C. § 103(a) because a *prima facie* case of obviousness has not been made by the Examiner.

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims (See M.P.E.P. § 2143.03 (8th ed. 2001).) Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art to combine the referenced in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of these requirements must "be found in the prior art, and not be based on applicant's disclosure" (See M.P.E.P. § 2143 (8th ed. 2001)).

The Examiner asserts that Applicants presented a piecemeal analysis in the response filed September 19, 2002 and that "Applicants did not provide any reason why

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the combined teachings do not render the claims obvious" (see Office Action, page 6, lines 12-15 and page 17-20). Applicants respectfully disagree. As mentioned above, to establish a prima facie case of obviousness, the Examiner must show that the references, alone or in combination, teach and/or suggest every step recited in claim 1, as well as provide evidence of some suggestion or motivation to combine the references in a manner resulting in the claimed invention. Accordingly, the September 19, 2002 response includes arguments that not only expose the deficiencies of each of the cited references in failing to teach or suggest each and every one of the steps recited in claim 1, but also presents arguments explaining why one of ordinary skill in the art would not have been motivated to combine the process of curing polymers, as taught by Lau et al., with the teachings of Ye et al. to render claim 1 obvious (see the Response filed September 19, 2002, page 4, lines 2-15). Contrary to the Examiner's position, Applicants arguments included in the September 19, 2002 response do not merely attack the references individually, but instead indicate why one of ordinary skill in the art would not have been motivated to combine the references to achieve at least the shrinking and forming steps included in claim 1. Accordingly, Applicants continue the same analysis below to establish that Ye et al. and Lau et al., alone or in combination, fail to teach or suggest the method recited in claim 1.

The Examiner asserts that Ye et al. teaches all of the steps of claim 1 and admits that Ye et al. does not specifically mention except for shrinking the low-dielectric pattern. Accordingly, because Ye et al. does not teach the shrinking step, it also cannot teach forming gate electrodes by patterning the conductive layer and the gate insulation layer *using the shrunken low-dielectric pattern as a mask*, as claimed (emphasis

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added). The Examiner, however, asserts that it would have been obvious to combine the curing process taught by Lau et al. with the method disclosed by Ye et al. to render claim 1 unpatentable under 35 U.S.C. § 103(a). Applicants disagree.

As explained, the curing process taught by Lau et al., and referred to by the Examiner, has no relation to a pattern layer used in the creation of a gate electrodes as recited in claim 1. Instead, the cured film described by Lau et al. in col. 14, lines 23-50 is associated with a process for cross linking polymers. The process described in col. 14 includes dissolving a polymer in a solvent and filtering the dissolved liquid on a glass plate. The coated plate is exposed to high temperatures for "curing" and forming a resulting film that may be peeled off the glass plate. Accordingly, Lau et al. does not teach, or even suggest, shrinking the low dielectric pattern and forming gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask, as recited in claim 1.

Further, neither Ye et al. or Lau et al. include any teaching or suggestion of a step of shrinking a low-dielectric pattern and using the shrunken pattern as a mask to form gate electrodes. Accordingly, one of ordinary skill in the art would not have been motivated to combine the teachings of Lau et al. with the process taught by Ye et al. to arrive at the steps of claim 1 because a teaching of a general curing of materials, including a polymer spun on a glass plate as disclosed by Lau et al., does not teach or suggest, at least, shrinking of a low-dielectric pattern as recited in claim 1.

Further, according to the Examiner, one of ordinary skill in the art would apply the curing process taught by Lau et al. to "cross-link the polymers of the low-dielectric layer" taught by Ye et al. (see Office Action, page 8, lines 2-9). Cross -linking polymers is not

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the same as shrinking a low-dielectric pattern that is used as a mask to form gate electrodes, as is done in the method of claim 1. The Examiner did not present any evidence of a reason or motivation, in any of the references themselves, why Ye et al. would desire to cross-link any of its polymers. Accordingly, the Examiner has not established a *prima facie* case of obviousness in rejecting claim 1.

Also, the Examiner asserts that the method for curing the dielectric pattern taught by Ye et al. to cross-link the polymers is "conveniently controllable with stable cross linking sites and do not introduce undesirable functionalities into the polymetric composition being cross linked." (see Office Action, page 8, lines 7-9). This assertion does not address why one of ordinary skill in the art would have been motivated to shrink the low-dielectric pattern and use the shrunken pattern as a mask, as recited in claim 1. Instead, the Examiner's assertion merely focuses on a method of performing the cross-linking to prevent some unidentified "undesirable functionalities." The Examiner has not provided any factual support for these assertions. Additionally, the Examiner contends that the motivation to combine Lau et al. and Ye et al. to result in the method recited in claim 1 is supported by the relationship between the technologies discussed in these references (i.e., same field of endeavor). The fact that Lau et al. discusses the use of polymers in layered circuitry does not provide a motivation to shrink a low-dielectric pattern for use as a mask for forming gate electrodes, as recited in claim 1. The reasons for curing polymers, as taught by Lau et al., have no relationship with reducing the size of a pattern mask to produce gate electrodes.

Further, assuming Lau et al. and Ye et al. were from the same field of endeavor (which Applicants do not concede), the fact that two references are related in

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technology is not alone a showing that there is motivation to combine the references for obviousness purposes. Although analogous art may be a factor in determining whether one reference may be properly combined with another to reject a claim under 35 U.S.C. § 103(a), the Examiner must still meet the requirement of providing evidence of a suggestion or motivation for the combination that is either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. Applicants respectfully submit that the Examiner has not made this showing.

Because Ye et al. and Lau et al., alone or in combination, fail to teach or suggest all of the steps of claim 1, Applicants request that the rejection of this claim under 35 U.S.C. § 103(a) be withdrawn and the claim allowed.

Claim 6 includes recitations similar to those of claim 1. As explained, claim 1 is distinguishable from Ye et al. and Lau et al. Accordingly, claim 6 is also distinguishable for at least the same reasons set forth for claim 1, and Applicants request that the rejection of this claim under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Claims 2-5 and 7-10 depend from claims 1 and 6, respectively. As explained, claims 1 and 6 are distinguishable from Ye et al. and Lau et al. Accordingly, claims 2-5 and 7-10 are also distinguishable from these references and Applicants request that the rejection of these claims under 35 U.S.C. § 103(a) be withdrawn and the claims allowed.

Applicants respectfully request that this Amendment under 37 C.F.R. § 1.116 be entered by the Examiner, placing claims 1-10 in condition for allowance. Applicants submit that the proposed amendments of claims 6 and 8 do not raise new issues or necessitate the undertaking of any additional search of the art by the Examiner, since all

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of the elements and their relationships claimed were inherent in the claims as examined. Therefore, this Amendment should allow for immediate action by the Examiner.

Furthermore, Applicants respectfully point out that the final action by the Examiner presented some new arguments as to the application of the art against Applicant's invention. It is respectfully submitted that the entering of the Amendment would allow the Applicants to reply to the final rejections and place the application in condition for allowance.

Finally, Applicants submit that the entry of the amendment would place the application in better form for appeal, should the Examiner dispute the patentability of the pending claims.

In view of the foregoing remarks, Applicants submit that this claimed invention, as amended, is neither anticipated nor rendered obvious in view of the prior art references cited against this application. Applicants therefore request the entry of this Amendment, the Examiner's reconsideration and reexamination of the application, and the timely allowance of the pending claims.

If there is any fee due in connection with the filing of this response, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER, L.L.P.

Dated: February 28, 2003

By: _____

Joseph E. Palys
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APPENDIX OF CLAIM AMENDMENTS

Please amend claims 6 and 8 as indicated in the attached Appendix and as presented below:

6. (Amended) A method for forming fine patterns of a semiconductor device, the method comprising:

forming a [material] patterning layer over a semiconductor wafer;

forming a low-dielectric layer over the [material] patterning layer;

forming a photoresist pattern whose width is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

removing the photoresist pattern;

shrinking the low-dielectric pattern; and

forming the fine patterns by patterning the [material] patterning layer using the shrunken low-dielectric pattern as a mask.

8. (Amended) The method of claim 6 or 7, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the [material] patterning layer for the fine patterns; and

soft-baking the low-dielectric layer at a predetermined temperature.



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